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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/966,095
Filing Date: October 01, 2001
Appellant(s): BALAY ET AL.

Bollman
For Appellant

EXAMINER'S ANSWER

This is in response to the (**corrected**) appeal brief filed 2/27/2007 appealing from the Office action mailed 7/28/2006

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,457,091 Lange et al. 09-2002

"Lucent Technologies Delivers New Fixed Programmable System Chips" (Lucent Technologies), 11/08/1999.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 6- 8, 10-12, 15-17, 19-21, 24- 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tal in view of Lucent Technologies.

With regard to claim 1, Tal discloses a system for interconnecting two or more computer bus architectures (the compact PCI (Peripheral Component Interconnect) shown generally at Fig. 8, for example), comprising: a first bus segment (PCI bus

segment 802, column 6, lines 43-64, for example) to transmit data information, a first half bridge circuit (the PCI serializer on system card 810 in segment 802, Fig. 8, and shown in details as PCI serializer 700 on segment 802, Fig. 7, column 6, lines 28-38; note that the extra serializer in card 806 on PCI bus segment 802, showed in Fig. 8, are only for redundancy; note also that the circuit 700, Fig. 7, corresponds to the half bridge disclosed by the Applicant in the originally filed specification, page 1, lines 12-17; page 6, lines 20-26, page 7, line 1 to page 9, line 4; and particularly Fig. 2.) connected to said first bus segment (PCI bus segment 802, column 6, lines 43-64, for example), said first half bridge circuit (PCI serializer 700, shown at Fig. 7, on segment 802 side, Fig. 8) comprising a first DMA circuit (704, Fig. 7, column 6, lines 28-28); a second bus segment (PCI bus segment 804, column 6, lines 43-64, for example) to transmit data information; a second half bridge circuit (the PCI serializer on card 812 in segment 804, Fig. 8, and shown in details as PCI serializer 700 on segment 804, Fig. 7, column 6, lines 28-38; note that the extra serializer in card 808 on PCI bus segment 804, showed in Fig. 8, are only for redundancy) connected to said first half bridge circuit (700, shown at Fig. 7, on segment 802 side), said second half bridge circuit (700, shown at Fig. 7, on segment 804 side) comprising a second DMA circuit (704, Fig. 7) and transferring data information between said first bus segment (segment 802, column 6, lines 43-64, for example), and said second bus segment (segment 804, column 6, lines 43-64, for example). Tal further discloses that the serial channel (having a plurality of data paths connecting the first half bridge to the second half bridge) is built out of 4 full duplex pairs, each providing 622 mbps of bandwidth. See column 6, lines 18-27. As disclosed

by the Applicants in the originally filed specification, page 6, lines 5-8, and lines 20-26, "the first half bridge circuit 4 is connected with the second half bridge circuit 6 by four full duplex high speed serial data lines 5 each having a bandwidth of 622 Mb/s" (emphasis added).

However, Tal does not disclose that the serial channel comprising 4 full duplex pair can be "scalable" depending on a bandwidth needed for a particular application. To define the term "scalable", Applicants cited page 10, lines 6-10 of originally filed specification, which states that "[a]lthough the present invention is described with reference to embodiments teaching four high speed serial data lines running between two half bridge circuits, the principles of the present invention are equally applicable to the addition or subtraction of high speed serial data lines depending upon the bandwidth needed between two half bridge circuits."

Lucent Technologies discloses the use of the ORT4622 half bridge (page 1, 4th paragraph) including field programmable gate arrays (FPGAs), see page 1, 1st paragraph, and containing "a 4-channel 622 megabit-per-second (2.5 gbps when all 4 channels are used), see page1, 4th paragraph, for providing design flexibility, functionality, and performance. See page 1, 1st and 5th paragraphs. The ORT4622 half bridge is clearly "scalable" depending on the bandwidth needed. The fact that the ORT4622 half bridge contains "a 4-channel 622 megabit-per-second (2.5 gbps when all 4 channels are used)" (emphasis added) clearly indicates that less than 4 channels can be used when less bandwidth is needed. As a matter of fact, the Lucent Technologies' ORT4622 half bridge is the same ORT4622 half bridge that Applicants employ.

Applicants clearly disclose that "[t]he first and second half bridge circuits, 4 and 6, would consist of an ORT4622 Lucent FPSC (Field Programmable System Chip) which implements a 2.5 Gb/s physical (LVDS Serial I/Os with clock recovery) and transport layers together with a PCI controller. Although the ORT4622 is shown, any number of components supporting high speed data transfer between bus segments could be used to implement the invention." See Figs 1 and 2, and Applicants' originally filed specification, page 6, lines 20-26. Since the Lucent Technologies' ORT4622 half bridge is the same ORT4622 half bridge that Applicants employ, it is clear that the serial data paths provided by the two ORT4622 half bridges are "scalable" depending on a bandwidth needed.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to employ the ORT4622 half bridge, as taught by Lucent Technologies, to replace the half bridge 700 (Figs. 7 and 8) on each side of the PCI bus segments of Tal, for the purpose of providing Tal with design flexibility/scalability, functionality, and speed/performance. See Lucent Technologies, page 1, 1st and 5th paragraphs.

With regard to claim 2, it is clear that segment 802 is a PCI architecture bus.

With regard to claim 3, it is clear that segment 804 is a PCI architecture bus.

With regard to claim 6, the first bus segment operates at a substantially same bus frequency as a bus frequency of said second bus segment (see column 4, line 61 to column 5, line 5; column 6, lines 18-27).

With regard to claims 7, 16, and 25, the ORT4622 half bridge includes field programmable gate arrays (FPGAs), see page 1, 1st paragraph, and 4th paragraph.

With regard to claim 8, the first half bridge circuit and said second half bridge circuit recover a clock signal from, respectively said first bus segment and said second bus segment (see at least column 6, lines 52-64). In any event, since the Lucent Technologies' ORT4622 half bridge is the same ORT4622 half bridge that Applicants employ (see page 6, lines 20-26), it is clear that the first half bridge circuit and said second half bridge circuit recover a clock signal from, respectively said first bus segment and said second bus segment.

With regard to claims 10-12, 15-17, see discussion above regarding claims 1-3, 6, and 8.

With regard to claims 19-21, 24-26, see discussion above regarding claims 1-3, 6, and 8.

Claims 5, 14, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tal, as applied to claims 1-3, 6- 8, 10-12, 15-17, 19-21, 24- 26 above, and further in view of the following.

Tal, as discussed above, discloses the claimed invention. Tal does not disclose that the bus operating frequencies of PCI bus segment (802) and PCI bus segment (804) may be different. However, the use of two PCI buses having different frequencies is old and well-known as evidenced by at least Lange et al. Lange clearly discloses that the bridge (PCI bridge connected to PCI buses according to PCI specification) can have

a bus width of either 32 bits or 64 bits. See at least column 3, lines 54-60. According to the PCI specification, PCI is operated at 33 MHz using a 32-bit-wide path; and the speed can be increased from 33 MHz to 66 MHz and the bit count can be doubled to 64. Currently, PCI-X provides for 64-bit transfers at a speed of 133 MHz.

Bus Type	Bus Width	Bus Speed	MB/sec
ISA	16 bits	8 MHz	16 MBps
EISA	32 bits	8 MHz	32 MBps
VL-bus	32 bits	25 MHz	100 MBps
VL-bus	32 bits	33 MHz	132 MBps
PCI	32 bits	33 MHz	132 MBps
PCI	64 bits	33 MHz	264 MBps
PCI	64 bits	66 MHz	512 MBps
PCI	64 bits	133 MHz	1 GBps

From the table above, it is clear that the buses can be operated under different speed, either 33 Mhz or 66 Mhz.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use two PCI buses having different frequencies, since the Examiner takes Official Notice that the use of two PCI buses having different frequencies is old and well-known as evidenced by at least Lange et al, and providing Tai with two PCI buses having different frequencies only involves ordinary skill in the art.

Claims 1-3, 5, 7, 8, 10-12, 14, 16, 17, 19-21, 23, 25, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lange et al. in view of Lucent Technologies.

With regard to claims 1-3, Lange discloses a system for interconnecting two or more computer bus architectures, comprising: a first bus segment (primary PCI bus 12, Figs. 2 and 4) to transmit data information; a first half bridge circuit (126, Figs. 2 and 4, column 5, lines 45-55) connected to the first bus segment (primary PCI bus 12, Figs. 2 and 4); a second bus segment (secondary PCI bus 14, Figs. 2 and 4) to transmit data information; a second half bridge circuit (127, Fig. 2, column 5, lines 45-55) connected to the first half bridge circuit (126, Figs. 2 and 4, column 5, lines 45-55) and the second bus segment (secondary PCI bus 14, Figs. 2 and 4) for transferring data information between the first half bridge circuit (126, Figs. 2 and 4, column 5, lines 45-55) and the second bus segment (secondary PCI bus 14, Figs. 2 and 4). In addition, Lange et al. also discloses that the first half bridge segment (12) and the second half bridge segment (14) communicate with a high speed serial line protocol (see at least col. 5, lines 49-51). Note that the serial line protocol includes a plurality of signal lines or data paths, see at least Fig. 2.

However, Lange does not disclose that the signal lines (provided by serial line protocol, see at least col. 5, lines 49-51, and Fig. 2) are "scalable" depending on a bandwidth needed for a particular application. To define the term "scalable", Applicants cited page 10, lines 6-10 of originally filed specification, which states that "[a]lthough the present invention is described with reference to embodiments teaching four high speed

serial data lines running between two half bridge circuits, the principles of the present invention are equally applicable to the addition or subtraction of high speed serial data lines depending upon the bandwidth needed between two half bridge circuits." See Appeal Brief, Summary of the Invention, last three lines.

Lucent Technologies discloses the use of the ORT4622 half bridge (page 1, 4th paragraph) including field programmable gate arrays (FPGAs), see page 1, 1st paragraph, and containing "a 4-channel 622 megabit-per-second (2.5 gbps when all 4 channels are used), see page1, 4th paragraph, for providing design flexibility, functionality, and performance. See page 1, 1st and 5th paragraphs. The ORT4622 half bridge is clearly "scalable" depending on the bandwidth needed. The fact that the ORT4622 half bridge contains "a 4-channel 622 megabit-per-second (2.5 gbps when all 4 channels are used)" (emphasis added) clearly indicates that less than 4 channels can be used when less bandwidth is needed. As a matter of fact, the Lucent Technologies' ORT4622 half bridge is the same ORT4622 half bridge that Applicants employ. Applicants clearly disclose that "[t]he first and second half bridge circuits, 4 and 6, would consist of an ORT4622 Lucent FPSC (Field Programmable System Chip) which implements a 2.5 Gb/s physical (LVDS Serial I/Os with clock recovery) and transport layers together with a PCI controller. Although the ORT4622 is shown, any number of components supporting high speed data transfer between bus segments could be used to implement the invention." See Figs 1 and 2, and Applicants' originally filed specification, page 6, lines 20-26. Since the Lucent Technologies' ORT4622 half bridge is the same ORT4622 half bridge that Applicants employ, it is clear that the serial data

paths provided by the two ORT4622 half bridges are "scalable" depending on a bandwidth needed.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to employ the ORT4622 half bridge, as taught by Lucent Technologies, to replace the half bridge 126 and 127 on each side of the PCI bus segments of Lange, for the purpose of providing Lange with design flexibility/scalability, functionality, and speed/performance. See Lucent Technologies, page 1, 1st and 5th paragraphs.

With regard to claims 5, 14, 23, Lange clearly discloses that the bridge (PCI bridge connected to PCI buses according to PCI specification) can have a bus width of either 32 bits or 64 bits. See at least column 3, lines 54-60. According to the PCI specification, PCI is operated at 33 MHz using a 32-bit-wide path; and the speed can be increased from 33 MHz to 66 MHz and the bit count can be doubled to 64. Currently, PCI-X provides for 64-bit transfers at a speed of 133 MHz.

Bus Type	Bus Width	Bus Speed	MB/sec
ISA	16 bits	8 MHz	16 MBps
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PCI	64 bits	66 MHz	512 MBps
PCI	64 bits	133 MHz	1 GBps

From the table above, it is clear that the buses can be operated under different speed, either 33 Mhz or 66 Mhz.

With regard to claims 7, 16, and 25, the ORT4622 half bridge includes field programmable gate arrays (FPGAs), see page 1, 1st paragraph, and 4th paragraph.

With regard to claims 8, 17, and 26, since the Lucent Technologies' ORT4622 half bridge is the same ORT4622 half bridge that Applicants employ (see page 6, lines 20-26), it is clear that the first half bridge circuit and said second half bridge circuit recover a clock signal from, respectively said first bus segment and said second bus segment.

With regard to claims 10-12, 14, 18, see discussion above.

With regard to claims 19-21, and 23, see discussion above.

Claims 6, 15, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lange et al., 1-3, 5, 7, 8, 10-12, 14, 16, 17, 19-21, 23, 25, and 26, and further in view of the following.

Lange et al., as discussed above, discloses the claimed invention. Lange et al. does not disclose that the bus operating frequencies of PCI bus (2) and PCI bus (4) may be substantially the same. However, the use of two PCI buses having substantially same frequencies is old and well-known as evidenced by at least Tal. Tal discloses that the first PCI bus segment operates at a substantially same bus frequency as a bus

frequency of said second PCI bus segment (see column 4, line 61 to column 5, line 5; column 6, lines 18-27).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use two PCI buses having substantially same frequencies, since the Examiner takes Official Notice that the use of two PCI buses having substantially same frequencies is old and well-known as evidenced by at least Tal (see column 4, line 61 to column 5, line 5; column 6, lines 18-27); and therefore, providing Lange et al. with two PCI buses having substantially same frequencies only involves ordinary skill in the art.

(10) Response to Argument

(A) Claims 1-3, 6-8, 10-12, 15-17, 19-21, and 24-26 are obvious under 35 USC 103(a) over Tal in view of Lucent Technologies.

Appellants argued that "[t]he Examiner relied on Lucent to allegedly disclose scalability. However, Lucent discloses that 'Designers can use the device to drive high-speed data transfer across a backplane within a system' (see 4th full paragraph). Thus, a reading of Lucent reveals that the manufacturer of the ORT4622 intended its use across a backplane within a system. Although Applicants also disclose use of the ORT4622, Applicants disclose a novel use of a feature of the ORT4622 that is not disclosed as being used by Lucent within a backplane. The Examiner has still failed to provide a reference that discloses or suggests the use of scalable half bridge circuits

between two bus segments, as recited by claims 1-3, 5-8, 10-12, 14-17, 19-21 and 23-26."

In response to Appellants' argument, at the outset, it is important to note that Appellants conceded that the Lucent Technologies' OR14622 half bridge is the same OR14622 half bridge that the Appellants employ.

Since the Lucent Technologies' ORT4622 is employed by Appellants to provide "scalability," it is also important to note that Applicants also conceded that Lucent Technologies discloses the scalability of the OR74622 half bridge.

Appellants also conceded that the ORT4622 is used "to drive high speed data transfer across a backplane within a system, such as a PCI-to-PCI half bridge." See Lucent Technologies, 4th paragraph.

Contrary to Appellants' argument, it is not understood what may be "a novel use of a feature of the ORT4622 that is not disclosed as being used by Lucent within a backplane." As a matter of fact, Appellants' originally filed specification reveals that the ORT4622 is used as a PCI-to-PCI half bridge, each is provided on a backplane to provide high speed data transfer between a first back plane structure and a second backplane structure; wherein each backplane contains a PCI bus segment and a plurality of PCI slots fro PCI cards. Note also that as defined in Compact PCI specification, a backplane is a circuit board containing a segment of PCI bus and a plurality of PCI slots for PCI cards. See Appellants' specification, page 1, lines 5-14, page 5, lines 7-15, and Fig. 1. Appellants' Fig. 1 is reproduced below:

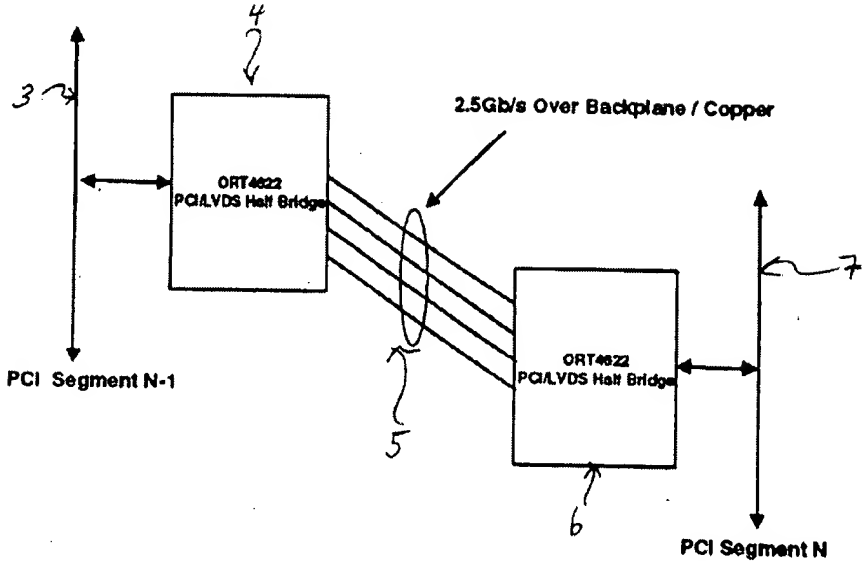

FIG. 1

Note the term "Over Backplane" used in Appellants' Fig. 1 above.

Thus, it is clear that **identical to Appellants' disclosure and claims**, Lucent Technologies discloses that the ORT4622 can be used as a PCI-to-PCI half bridge. Note that the Lucent OR74622 PCI-PCI half bridge, as its name implies, has to be employed **in pair.** Instead of using a PCI bridge connecting the two PCI buses, one can use a half PCI bridge, each connected to a respective PCI bus. Thus, 1 PCI bridge = 2 X half PCI bridges. As a matter of fact, it is well-defined in the field of computer architecture that a half bridge is used in pair. For example, US Patent No. 6,687,779 (cited in previous Office Action as relevant art) discloses the use of a PCI half bridge that can be used a primary or secondary part of a PCI bridge. Each half bridge is connected to a respective PCI bus (see at least column 3, line 66 to column 4, line 5). Another example is the disclosure of US Patent No. 6,968,464 (cited in previous Office

Action as relevant art) describing the use of a pair of PCI half bridge as disclosed in US Patent No. 6,070,214. Specifically, US Patent No. 6,968,464 discloses that "U.S. Pat. No. 6,070,214 assigned to Mobility Electronics also describes a "split bridge" implementation. A split bridge may allow the extension of a computer bus, such as a PCI bus, to a remote location with little or no performance degradation or software requirements. For example, standard PCI--PCI bridge chip functionality may be split between two remotely located components which may be located on the computer and the remote chassis, respectively. For example, in a PCI split bridge system, the host computer includes a primary PCI bus and a first interface comprising a first portion of the bridge, the remote system includes a secondary PCI bus and a second interface comprising a second portion of the bridge, and the two systems are coupled via a transmission medium, e.g., a serial or parallel transmission cable. The first interface, the transmission medium, and the second interface may collectively comprise the bridge. In this manner, PCI devices attached to both of the PCI systems may be coupled seamlessly, or transparently, i.e., the PCI expansion devices coupled to the remote PCI bus may appear to the computer system as if they were coupled directly to the local PCI bus in the host computer system. One added benefit of this approach is the expansion of the number of PCI devices which may be included in the overall system, normally limited to 3 or 4 PCI devices. Of course, this technique is not limited to PCI based systems, and may be used with other buses as well, such as Compact PCI, PXI, VME or VXI, among others" (see column 2, lines 20-47). Thus, identical to Appellants' disclosure and claims, it is clear that the Lucent ORT4622 PCI

half bridge is used in pair, each ORT4622 PCI half bridge is connected to a first PCI bus segment and a second PCI bus segment of Tal.

Appellants also argued that "the motivation that the Examiner provided to modify Tal is to provide Tal 'with design flexibility/scalability, functionality, and speed performance' that the Examiner acknowledged is disclosed by Lucent (see Final Office Action dated July 28, 2006, pages 6 and 11). Thus, the Examiner is simply reiterating benefits from a marketing statement associated with the ORT4622 not providing motivation why one or ordinary skill would modify Tal. Moreover, the Applicants pointed out that 'Teachings of references can be combined only if there is some suggestion or incentive to do so.' In re Fine, 5 USPQ2d 1596,1600 (Fed. Cir. 1988) (quoting ACS Hosp. Sys. v. Montefiore Hosp., 221 USPQ 929, 933 (Fed. Cir. 1984)) (emphasis in original). Nothing within Tal nor Lucent suggests modifying Tal with scalable half-bridge circuits. Thus, any modification of Tal without some suggestion for such a modification is based on improper hindsight."

In response to Appellants' argument, at the outset, it is noted that Appellants conceded that Lucent Technologies' ORT4622 discloses that the ORT4622 provides design flexibility/scalability, functionality, and speed performance.

It is also noted that whether the design benefit/advantage (motivation) disclosed by Lucent Technologies is the so-called "marketing statement" as alleged by Appellants, is irrelevant.

In any event, Contrary to Appellants' argument, the motivation for the combination of Tal and Lucent ORT4622 half bridge is clearly set forth in the 35 USC

103 rejection. As clearly stated in the rejection, "It would have been obvious to one of ordinary skill in the art at the time the invention was made to employ the ORT4622 half bridge, as taught by Lucent Technologies, to replace the half bridge 700 (Figs. 7 and 8) on each side of the PCI bus segments of Tal, for the purpose of providing Tal with design flexibility/scalability, functionality, and speed/performance. See Lucent Technologies, page 1, 1st and 5th paragraphs" (emphasis added). Appellants are also reminded that obviousness can be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988), and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, as stated above, it is clear that the motivation for the combination of Tal and Lucent ORT4622 half bridge is clearly set forth in the 35 USC 103 rejection. Further, as set forth in MPEP Section 2144, "the strongest rationale for combining references is a recognition, expressly or impliedly in the prior art or drawn from a convincing line of reasoning based on established scientific principles or legal precedent, that some advantage or expected beneficial result would have been produced by their combination. *In re Sernaker*, 702 F.2d 989, 994-95, 217 USPQ 1, 5-6 (Fed. Cir. 1983)." In the instant case, the advantage or expected beneficial result, which would have been produced by the combination, is design flexibility/scalability, functionality, and speed/performance.

Appellants also argued that "as the Examiner points out Tal discloses reliance on 4 full duplex pairs, each providing 622 mbps of bandwidth at page 6, lines 18-27 (see Final Office Action dated July 28, 2006, page 4). Thus, Tal teaches away from modification to use a scalable interface because it specifically requires use of all four full duplex pairs for his application to provide "a bandwidth that will not hinder the eight slot per segment cPCI bus" (see col. 6, lines 18-19).

In response to Appellants' argument, at the outset, the portion of Tai, in its full context, is reproduced below:

"Preferably, the serial channel provides a bandwidth that will not hinder the eight slot per segment CPCI [Compact PCI] bus. The serial channel is built out of 4 full duplex pairs, each providing 622 mbps of bandwidth" (emphasis added). See column 6, lines 18-27.

From the portion quoted above, it is clear that Tal only discloses that preferably, the serial channel built from 4 full duplex pairs, each providing 622 mbps of bandwidth, would provide sufficient bandwidth when all eight PCI slots involves in data transfer. In other words, in Tal, the serial channel comprising 4 full duplex pairs, each providing 622 mbps of bandwidth, is preferable when all eight PCI slots in the CPCI bus segment is used. Note that each CPCI bus segment is provided with a maximum of eight PCI slots for eight PCI cards. Note also that, identical to the disclosure of Tal, as disclosed by the Applicants in the originally filed specification, page 6, lines 5-8, and lines 20-26, "the first half bridge circuit 4 is connected with the second half bridge circuit 6 by four full duplex high speed serial data lines 5 each having a bandwidth of 622 Mb/s" (emphasis added).

What Tal does not disclose is that the serial channel is scalable if less bandwidth (less number of PCI slots involves in data transfer) is needed depending on a particular application. Thus, contrary to Appellants' argument, it is clear that Tal does not at all teaches away from modification to use a scalable interface. Appellants are also reminded that the Rejection is a 35 USC 103(a) Rejection based on a combination of references, wherein the Tal reference is used as a primary reference. The "scalability" which is not disclosed by Tal (primary) is clearly taught by Lucent Technologies (Secondary). Lucent Technologies discloses the use of the ORT4622 half bridge (page 1, 4th paragraph) including field programmable gate arrays (FPGAs), see page 1, 1st paragraph, and containing "a 4-channel 622 megabit-per-second (2.5 gbps when all 4 channels are used), see page1, 4th paragraph, for providing design flexibility, functionality, and performance. See page 1, 1st and 5th paragraphs. The ORT4622 half bridge is clearly "scalable" depending on the bandwidth needed. The fact that the ORT4622 half bridge contains "a 4-channel 622 megabit-per-second (2.5 gbps when all 4 channels are used)" (emphasis added) clearly indicates that less than 4 channels can be used when less bandwidth is needed. As a matter of fact, the Lucent Technologies' ORT4622 half bridge is the same ORT4622 half bridge that Applicants employ. Applicants clearly disclose that "[t]he first and second half bridge circuits, 4 and 6, would consist of an ORT4622 Lucent FPSC (Field Programmable System Chip) which implements a 2.5 Gb/s physical (LVDS Serial I/Os with clock recovery) and transport layers together with a PCI controller. Although the ORT4622 is shown, any number of components supporting high speed data transfer between bus segments could be used

to implement the invention." See Figs 1 and 2, and Applicants' originally filed specification, page 6, lines 20-26. Since the Lucent Technologies' ORT4622 half bridge is the same ORT4622 half bridge that Applicants employ, it is clear that the serial data paths provided by the two ORT4622 half bridges are "scalable" depending on a bandwidth needed. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ the ORT4622 half bridge, as taught by Lucent Technologies, to replace the half bridge 700 (Figs. 7 and 8) on each side of the PCI bus segments of Tal, for the purpose of providing Tal with design flexibility/scalability, functionality, and speed/performance. See Lucent Technologies, page 1, 1st and 5th paragraphs.

As discussed above, the rejection is based on a combination of references. One cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). As already conceded by Applicants that the Lucent PCI half bridge is scalable depending on a particular bandwidth, it is clear that the combination of Tal and Lucent ORT4622 PCI half bridge would provide a method and apparatus relying on a plurality of data paths used to connect a first half bridge circuit and a second half bridge circuit that are scalable depending on a bandwidth needed for a particular application.

(B) Claims 5, 14, and 23 are obvious under 35 USC 103(a) over Tal in view of Lange.

Appellants argued that "[t]he Examiner relied on Lange to allegedly disclose a bridge that can have a bus width of either 32 bits or 64 bits (see Office Action dated July 28, 2006, page 7). However, a reading of Lange reveals that the bridge the Examiner refers to is "used to decouple a processor and an expansion bus" (see Lange col. 3, lines 58-61). Thus, Lange "scalability" lacks any real relevance to Applicants' claimed features, i.e., Lange, like Tal, fails to disclose scalable half bridge circuits connecting a first bus segment and a second bus segment, as recited by claims 5, 14 and 23. Thus, Tal modified by Lange would at best theoretically result in Tal using a bus width of 32 bits or 64 bits "to decouple a processor and an expansion bus". Tal modified by Lange would still fail to disclose or suggest a first half bridge circuit and a second half bridge circuit connecting a first bus segment and a second bus segment, and a plurality of scalable data paths connecting the half bridge circuits, scalable dependent upon a bandwidth needed for a particular application, as recited by claims 5, 14 and 23."

Contrary to Appellants' argument, Lange clearly discloses that the bridge (PCI bridge connected to PCI buses according to the PCI architecture) can have a bus width of either 32 bits or 64 bits. See at least column 3, lines 54-60 of Lange. Note also that the PCI bridge, PCI-to-PCI half bridge, as well as Compact PCI must be all in full compliant with the PCI architecture. Lange is not relied upon by the Examiner for the disclosure of "scalability." Appellants are again reminded that, the rejection is based on a combination of references. One cannot show nonobviousness by attacking references

individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Further, Appellants argued that the Tal reference and Lange reference are not physically combined ("Tal modified by Lange would at best theoretically result in Tal using a bus width of 32 bits or 64 bits "to decouple a processor and an expansion bus"). In response to Appellants' argument, The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference. Rather, the test is what the combined teachings of those references would have suggested to those of ordinary skill in the art." *In re Keller*, 642 F.2d 413, 425, 208 USPQ 871, 881 (CCPA 1981). See also *In re Sneed*, 710 F.2d 1544, 1550, 218 USPQ 385, 389 (Fed. Cir. 1983) ("[I]t is not necessary that the inventions of the references be physically combinable to render obvious the invention under review."); and *In re Nievelt*, 482 F.2d 965, 179 USPQ 224, 226 (CCPA 1973) ("Combining the teachings of references does not involve an ability to combine their specific structures.").

(C) Claims 1-3, 5, 7, 8, 10-12, 14, 16, 17, 19-21, 23, 25, and 26 are obvious under 35 USC 103(a) over Lange in view of Lucent Technologies.

Appellants argued that "[t]he Examiner relied on Lucent to allegedly disclose scalability. However, as discussed above, Lucent discloses that 'Designers can use the device to drive high-speed data transfer across a backplane within a system' (see 4th full paragraph). Thus, a reading of Lucent reveals that the manufacturer of the

ORT4622 intended its use across a backplane within a system. Although Applicants also disclose use of the ORT4622, the Applicants disclose a novel use of a feature of the ORT4622 that is not disclosed as being used by Lucent within a backplane. The Examiner has still failed to provide a reference that discloses or suggests the use of scalable half bridge circuits between two bus segments, as recited by claims 1-3, 5, 7, 8, 10-12, 14, 16, 17, 19-21, 23, 25 and 26."

In response to Appellants' argument, at the outset, it is important to note that Appellants conceded that the Lucent Technologies' OR14622 half bridge is the same OR14622 half bridge that the Appellants employ.

Since the Lucent Technologies' ORT4622 is employed by Appellants to provide "scalability," it is also important to note that Applicants also conceded that Lucent Technologies discloses the scalability of the OR74622 half bridge.

Appellants also conceded that the ORT4622 is used "to drive high speed data transfer across a backplane within a system, such as a PCI-to-PCI half bridge." See Lucent Technologies, 4th paragraph.

Contrary to Appellants' argument, it is not understood what may be "a novel use of a feature of the ORT4622 that is not disclosed as being used by Lucent within a backplane." As a matter of fact, Appellants' originally filed specification reveals that the ORT4622 is used as a PCI-to-PCI half bridge, each is provided on a backplane to provide high speed data transfer between a first back plane structure and a second backplane structure; wherein each backplane contains a PCI bus segment and a plurality of PCI slots fro PCI cards. Note also that as defined in Compact PCI

specification, a backplane is a circuit board containing a segment of PCI bus and a plurality of PCI slots for PCI cards. See Appellants' specification, page 1, lines 5-14, page 5, lines 7-15, and Fig. 1. Appellants' Fig. 1 is reproduced below:

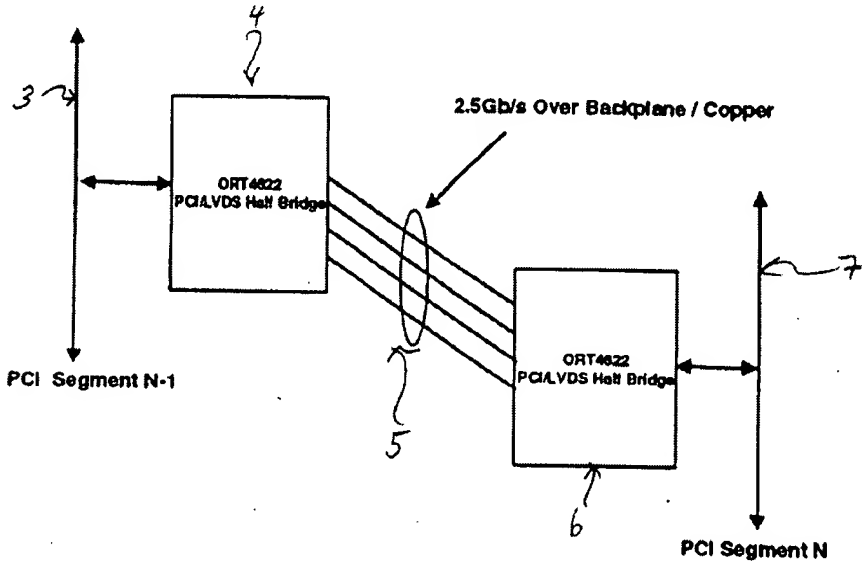

FIG. 1

Note the term "Over Backplane" used in Appellants' Fig. 1 above.

Thus, it is clear that **identical to Appellants' disclosure and claims**, Lucent Technologies discloses that the ORT4622 can be used as a PCI-to-PCI half bridge. Note that the Lucent OR74622 PCI-PCI half bridge, as its name implies, has to be employed **in pair.** Instead of using a PCI bridge connecting the two PCI buses, one can use a half PCI bridge, each connected to a respective PCI bus. Thus, 1 PCI bridge = 2 X half PCI bridges. As a matter of fact, it is well-defined in the field of computer architecture that a half bridge is used in pair. For example, US Patent No. 6,687,779 (cited in previous Office Action as relevant art) discloses the use of a PCI half bridge

that can be used a primary or secondary part of a PCI bridge. Each half bridge is connected to a respective PCI bus (see at least column 3, line 66 to column 4, line 5). Another example is the disclosure of US Patent No. 6,968,464 (cited in previous Office Action as relevant art) describing the use of a pair of PCI half bridge as disclosed in US Patent No. 6,070,214. Specifically, US Patent No. 6,968,464 discloses that "U.S. Pat. No. 6,070,214 assigned to Mobility Electronics also describes a "split bridge" implementation. A split bridge may allow the extension of a computer bus, such as a PCI bus, to a remote location with little or no performance degradation or software requirements. For example, standard PCI--PCI bridge chip functionality may be split between two remotely located components which may be located on the computer and the remote chassis, respectively. For example, in a PCI split bridge system, the host computer includes a primary PCI bus and a first interface comprising a first portion of the bridge, the remote system includes a secondary PCI bus and a second interface comprising a second portion of the bridge, and the two systems are coupled via a transmission medium, e.g., a serial or parallel transmission cable. The first interface, the transmission medium, and the second interface may collectively comprise the bridge. In this manner, PCI devices attached to both of the PCI systems may be coupled seamlessly, or transparently, i.e., the PCI expansion devices coupled to the remote PCI bus may appear to the computer system as if they were coupled directly to the local PCI bus in the host computer system. One added benefit of this approach is the expansion of the number of PCI devices which may be included in the overall system, normally limited to 3 or 4 PCI devices. Of course, this technique is not

limited to PCI based systems, and may be used with other buses as well, such as Compact PCI, PXI, VME or VXI, among others" (see column 2, lines 20-47). Thus, identical to Appellants' disclosure and claims, it is clear that the Lucent ORT4622 PCI half bridge is used in pair, each ORT4622 PCI half bridge is connected to a first PCI bus segment and a second PCI bus segment of Lange.

Appellants also argued that "the motivation that the Examiner provided to modify Lange is to provide Lange 'with design flexibility/scalability, functionality, and speed performance' that the Examiner acknowledged is disclosed by Lucent (see Final Office Action dated July 28, 2006, pages 6 and 11). Thus, the Examiner is simply reiterating benefits from a marketing statement associated with the ORT4622 not providing motivation why one or ordinary skill would modify Lange. Moreover, the Applicants pointed out that 'Teachings of references can be combined only if there is some suggestion or incentive to do so.' In re Fine, 5 USPQ2d 1596,1600 (Fed. Cir. 1988) (quoting ACS Hosp. Sys. v. Montefiore Hosp., 221 USPQ 929, 933 (Fed. Cir. 1984)) (emphasis in original). Nothing within Lange nor Lucent suggests modifying Lange with scalable half-bridge circuits. Thus, any modification of Langé without some suggestion for such a modification is based on improper hindsight."

In response to Appellants' argument, at the outset, it is noted that Appellants conceded that Lucent Technologies' ORT4622 discloses that the ORT4622 provides design flexibility/scalability, functionality, and speed performance.

It is also noted that whether the design benefit/advantage (motivation) disclosed by Lucent Technologies is the so-called "marketing statement" as alleged by Appellants, is irrelevant.

In any event, Contrary to Appellants' argument, the motivation for the combination of Lange and Lucent ORT4622 half bridge is clearly set forth in the 35 USC 103 rejection. As clearly stated in the rejection, "it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ the ORT4622 half bridge, as taught by Lucent Technologies, to replace the half bridge 126 and 127 on each side of the PCI bus segments of Lange, for the purpose of providing Lange with design flexibility/scalability, functionality, and speed/performance. See Lucent Technologies, page 1, 1st and 5th paragraphs." Appellants are also reminded that obviousness can be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988), and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, as stated above, it is clear that the motivation for the combination of Lange and Lucent ORT4622 half bridge is clearly set forth in the 35 USC 103 rejection. Further, as set forth in MPEP Section 2144, "the strongest rationale for combining references is a recognition, expressly or impliedly in the prior art or drawn from a convincing line of reasoning based on established scientific principles or legal precedent, that some advantage or expected beneficial result would have been

produced by their combination. *In re Sernaker*, 702 F.2d 989, 994-95, 217 USPQ 1, 5-6 (Fed. Cir. 1983)." In the instant case, the advantage or expected beneficial result, which would have been produced by the combination, is design flexibility/scalability, functionality, and speed/performance.

Appellants also argued that "Lange discloses use of a single serial communication line (see Fig. 4, item 131). Thus, Lange teaches away from the Examiner's alleged modification of use of more than one data line that would add cost and complexity to his system because requiring use of only one data line for his application."

Contrary to Appellants' argument, item 131 (shown in Fig. 4 as a single line) is not a "single communication line" as alleged by Appellants. The drawing is only used for illustration purpose. Lange et al. discloses that the first half bridge segment (12) and the second half bridge segment (14) communicate with a high speed serial line protocol (see at least col. 5, lines 49-51). Note that the serial line protocol includes a plurality of signal lines or data paths, see at least Fig. 2. With regard specifically to serial communication bus 131, Lange discloses in column 7, lines 1-16 that:

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Serial interconnection bus circuitry **130** and **132** each comprise FIFO queues **122**, **124** and **123**, **125**, respectively, and interface circuitry **160**, **162** and **161**, **163**, respectively (as shown in FIG. **2**). It is understood that serial interconnection bus circuitry **130** and **132** also each comprise transmitting and receiving circuitry included with interface circuitry **160**–**163** (of FIG. **2**) and operative to transmit and receive between primary portion **126** and secondary portion **127** of bus bridge **110**. It is also understood that serial interconnection bus circuitry **130** and **132** are signal coupled together via a serial communication link **131**, including connector **112**. Serial communication link **131** is removably connected via connector **112**, between bus circuitry **130** and **132**. In one form, serial communication link **131** forms a part of a serial bus, defined by bus circuitry **130**, **132** and communication link **131**.

(D) Claims 6, 15, and 24 are obvious under 35 USC 103(a) over Lange in view of Official Notice.

Appellants argued that "Official Notice was relied on to disclose two PCI buses having substantially same frequencies. Thus, Lange even in view of two PCI buses having substantially same frequencies still fails to disclose or suggest scalable signal lines between two half bridge circuits, i.e., Lange even in view of the unsupported Official Notice fails to disclose or suggest a method and apparatus relying on a first half bridge circuit and a second half bridge circuit connecting a first bus segment and a second bus segment, and a plurality of scalable data paths connecting the half bridge circuits, scalable dependent upon a bandwidth needed for a particular application, as recited by claims 6, 15 and 24."

At the outset, it is noted that "Official Notice" is not relied upon by the Examiner for the disclosure of "scalability." Appellants are again reminded that, the rejection is based on a combination of references. One cannot show nonobviousness by attacking

references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). The Official Notice (with supportive evidence provided) is relied upon for the fact that using two PCI buses having substantially same frequency is old and well-known in the art. As clearly stated in the 35 USC 103(a) Rejection over Lange in view of Lucent Technologies and further in view of "Official Notice," the Examiner takes Official Notice that the use of two PCI buses having substantially same frequencies is old and well-known as evidenced by at least Tal (see column 4, line 61 to column 5, line 5; column 6, lines 18-27).

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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Conferees:

See "Notice of Panel Decision from Pre-Appeal Brief Review."

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